REMARKS/ARGUMENTS

Claims 1-17 were pending in this application before submission of this paper. Claims 1-17 were rejected. Claims 1, 4, 5, 8, 11, 14, 16 and 17 are amended. Claims 2, 3 and 15 are cancelled. No new matter has been added. Claims 1, 4-14, 16 and 17 are currently pending. In view of the following remarks, reconsideration and allowance of all pending claims are respectfully requested.

Claims 1-3, 5, 8-10 and 14-15 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Tamches et al*, "Fine-grained Dynamic Instrumentation of Commodity Operating System Kernels." Claims 4, 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tamches et al.* in view of *Kiyohara et al.*, "Register Connection: A New Approach to Adding Registers into Instruction Set Architectures." Claims 11, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tamches et al.* in view of *Aho et al.*, "Compilers Principles, Techniques, and Tools." Claims 12 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tamches et al.* in view of *Aho et al.*, and in further view of *Tamches et al.* Applicants respectfully traverse these rejections.

Tamches et al. does not teach the limitations as recited in Applicants' amended Claim 1, including "generating a number of registers by adding the maximum number of registers and the additional number of registers; modifying the computer-executable binary to request the number of registers; and requesting the number of registers."

Tamches et al. teaches dynamic instrumentation steps including live register analysis and patch allocation to hold generated code. Live register analysis involves determining registers that are available for scratch use at the instrumentation point. (page 120, col. 2, pars. 3 & 4) *Tamches et al.* also teaches the assumption of a maximum number of instructions needed to perform a jump back to an instruction following an instrumentation point. (page 121, col. 1, par. 3) The teachings of *Tamches et al.* are different than the limitations recited in Applicants' Claim 1. Specifically, *Tamches et al.* does not teach "generating a number of registers by adding the maximum number of registers and the additional number of registers; modifying the computer-executable binary to request the number of registers; and requesting the number of registers." Thus, Claim 1 is proposed to be allowable and notice to that effect is solicited.

The Office Action rejected independent Claims 8 and 14 by citing essentially the same disclosures in *Tamches et al.* that were used to reject Claim 1. As discussed above, Claim 1, as amended, is proposed to be allowable. Applicants have amended Claims 8 and 14 to include the same limitation that placed Claim 1 in a state of allowability. Thus, Applicants respectfully submit that the invention taught by independent Claims 8 and 14 is not anticipated or rendered obvious by *Tamches et al.* and is proposed to be allowable.

As discussed above, independent Claims 1, 8 and 14 are proposed to be allowable. Thus, dependent Claims 4-7, 9-13, 16 and 17 are allowable for at least the same reasons that the base claims on which they rely are allowable, and notice to that effect is solicited.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

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